REMARKS/ARGUMENTS

In this amendment, claims 5 and 6 are amended and new claim 9 is added. Support can be found in the original claim 5 and paragraph [0016] of the present specification. Claims 1-4 are cancelled without prejudice. Now, claims 5-9 are pending. The Applicants submit currently pending claims 5-9 would not have been obvious over the cited references, i.e. Poirion and Kang, for the following reasons.

Re claims 5-8

The combined teachings of Poirion in view of Kang fail to disclose each of said first and said second read/write signals is a part of a specific read/write signal for obtaining a specified image data from said system memory to be processed by said graphics accelerator. According to the present invention, **the specified image data in the system memory is obtained by the graphics accelerator via at least two paths**, i.e. the first and second data transmission channels.

By contrast, in Poirion the graphics controller 5 (that is considered equivalent to the graphics accelerator of the present invention by the Examiner) accesses the frame buffer 18 through the frame buffer controller 15 (that is considered equivalent to the back-up memory control circuit of the present invention by the Examiner) and the frame buffer bus 17 (that is considered equivalent to the second data transmission channel of the present invention by the Examiner). The graphics controller need not share the system memory 9 with the processor, thus avoiding the memory sharing problems (col. 3, lines 57-64). In other words, the memory controller 4 and system bus 10 are not used by the graphics controller 5 in this case. In fact, the memory controller 4 and system bus 10 are used by the graphics controller 5 in the case that the frame buffer 18 is not present (col. 3, lines 50-56).

Basically, **only one path is used by Poirion's graphics accelerator to obtain the specified image data**, which is quite different from the present invention. Even though the access of the graphics controller to the system memory may be arranged to be available in Poirion, it is still hard to conclude that these two paths work together, particularly when Poirion fails to suggest the object of the present invention, i.e. the bandwidth enhancement for data transmission between the graphics accelerator and the system memory.

The Kang patent was cited only for the purpose of disclosing system memory and frame buffer into a unified system memory. Kang fails to disclose or suggest those claimed features missing in Poirion.

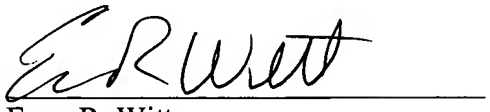
In view of the foregoing, the amended claim 5 and its dependent claims 6-8 would not have been obvious from the combined teachings of Poirion and Kang.

Re claim 9

The combined teachings of Poirion in view of Kang fail to disclose that the first and second data transmission channels transmit first and second portions of an image data from the frame buffer in the system memory in response to first and second read/write signals issued by the primary memory control circuit and the backup memory control circuit, respectively. According to Poirion, it is intended to use the single-chip chipset in both the configuration with a separate frame buffer and the configuration without a separate frame buffer. In the configuration with a separate fame buffer 18, the graphics controller 5 accesses the frame buffer 18 through the frame buffer controller 15 and the frame buffer bus 17 (col. 3, lines 57-64). On the other hand, in the configuration without a separate frame buffer 18, i.e. the frame buffer is disposed in the system memory, the graphic controller 15 accesses the shared system memory 9 through the memory controller 4 and the system bus 10, and the frame buffer controller 15 is not used (col. 3, lines 50-56). In other words, **in Poirion's configuration most similar to the present invention, i.e., the frame buffer is disposed in the system memory, Poirion only uses the memory controller 4 and the system bus 10, while the present invention, in contrast, uses both of the memory control circuits and data transmission channels**. As mentioned above, Kang fails to disclose or suggest those claimed features missing in Poirion. Applicants respectfully submit that claim 9 would not have been obvious from the combined teachings of Poirion and Kang.

Applicants respectfully submit that pending claims 5-8 are in condition for allowance and request that a timely Notice of Allowance be issued in this case. If there are any remaining issues preventing allowance of the pending claims that may be clarified by telephone, the Examiner is requested to call the undersigned.

Respectfully submitted,



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